Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	846	703/2.ccor.	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L2	314	703/13.ccor.	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L3	102	703/19.ccor.	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L4	468	716/2.ccor.	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L5	13	("6347393").URPN.	USPAT	OR	ON	2005/07/28 11:06
L6	2	("5841672" | "6117182").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/28 11:06
L7	592	716/6.ccor.	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/28 11:06
L8	6	(("6434729") or ("6347393") or ("6807659") or ("6868533") or ("6662149") or ("6615395")).PN.	US-PGPUB; USPAT	OR	OFF	2005/07/28 11:06
L9	6105	delay with model	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L10	1132	L9 and capacitance	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L11	44573	(interconnect path wir$3) with delay	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L12	738	L10 and L11	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L13	347	L12 and @ad<="20000922"	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L14	174	L13 and node	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L15	131	elmore adj delay	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L16	44	L13 and L15	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L17	3218	effective adj capacitance	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L18	296	L17 and moment	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L19	16	L18 and admittance	US-PGPUB; USPAT	OR	ON	2005/07/28 11:06
L20	8	("5617325" | "5675502" | "5841672" | "5872717" | "6014510" | "6047117" | "6314546" | "6347393").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/28 11:06
L21	9	("5469366" | "5761076" | "5787008" | "5790415" | "6314546" | "6347393" | "6353917" | "6496960" | "6510404").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/07/28 11:06

		Results
11.	pub-date > 1939 and pub-date < 2001 and FULL-TEXT(delay model) and FULL-TEXT(elmore) *[All Sources(- All Sciences -)]*	12
10.	pub-date > 1939 and pub-date < 2001 and FULL-TEXT(delay model) and FULL-TEXT(effective capacitance) *[All Sources(- All Sciences -)]*	4
9.	(pub-date > 1939 and pub-date < 2001 and FULL-TEXT((interconnect! delay or path delay or wir! delay)) and FULL-TEXT (moment)) and capacitance *[All Sources(- All Sciences -)]*	21
8.	pub-date > 1939 and pub-date < 2001 and FULL-TEXT((interconnect! delay or path delay or wir! delay)) and FULL-TEXT (moment) *[All Sources(- All Sciences -)]*	73
7.	(pub-date > 1939 and pub-date < 2001 and FULL-TEXT((interconnect! delay or path delay or wir! delay)) and FULL-TEXT (delay model)) and capacitance *[All Sources(- All Sciences -)]*	20
6.	pub-date > 1939 and pub-date < 2001 and FULL-TEXT((interconnect! delay or path delay or wir! delay)) and FULL-TEXT (delay model) *[All Sources(- All Sciences -)]*	35
5.	pub-date > 1939 and pub-date < 2001 and FULL-TEXT((interconnect! delay or path delay or wir! delay)) and FULL-TEXT (effective capacitance) *[All Sources(- All Sciences -)]*	2
4.	(((pub-date > 1939 and pub-date < 2001 and FULL-TEXT((interconnect! delay or path delay or wir! delay)) and FULL-TEXT(capacitance)) and model) and node) and effective *[All Sources(- All Sciences -)]*	29
3.	((pub-date > 1939 and pub-date < 2001 and FULL-TEXT((interconnect! delay or path delay or wir! delay)) and FULL-TEXT(capacitance)) and model) and node *[All Sources(- All Sciences -)]*	50
2.	(pub-date > 1939 and pub-date < 2001 and FULL-TEXT((interconnect! delay or path delay or wir! delay)) and FULL-TEXT (capacitance)) and model *[All Sources(- All Sciences -)]*	95
1.	pub-date > 1939 and pub-date < 2001 and FULL-TEXT((interconnect! delay or path delay or wir! delay)) and FULL-TEXT (capacitance) *[All Sources(- All Sciences -)]*	150

CiteSeer Find: effective capacitance and delay mo Documents Citations

Searching for **effective capacitance and delay model**.
Restrict to: Header Title Order by: Expected citations Hubs Usage Date Try: Google (CiteSeer) Google (Web) Yahoo! MSN CSB DBLP
8 documents found. **Order: number of citations.**

TACO: Timing Analysis With COupling - Arunachalam, Rajagopal, Pileggi (2000) (Correct) (11 citations)
Ceff **Delay Model** We use the coupled-gate **effective capacitance** (Ceff) model presented in [6] as the core on static timing analysis and the coupled **delay model** that we use. We formulate the coupled timing
www.sigda.org/Archives/ProceedingArchives/Dac/Dac2000/papers/2000/dac00/htmfiles/sun_sgi/../../pdffiles/16_3.pdf

Noise and Delay Uncertainty Studies for Coupled RC.. - Kahng, Muddu, Vidhani (1999) (Correct) (7 citations)
upon the switching conditions. A single **effective capacitance** value for the interconnect is computed ramp input. We also develop a simplified **delay model** for estimating delays on coupled RC lines interconnects. From Table 3 we see that our P **model delays** are close to the SPICE-computed values.
vlsicad.cs.ucla.edu/papers/conference/c100.ps

Capturing the Effect of Crosstalk on Delay - Sachin Sapatnekar Department (2000) (Correct) (2 citations)
2Cc is not a strict upper bound on the **effective capacitance**. In such a case, if a lower bound and be seen later, the only requirement that the **delay model** must satisfy is that an increase [decrease] in
www.ee.umn.edu/users/sachin/pubhtml/../PUBS/vlsi00.pdf

Repeater Insertion in Tree Structured Inductive Interconnect - Ismail, Friedman, Neves (2001) (Correct) (1 citation)
delay, moment matching methods, and/or the **effective capacitance** model to evaluate the insertion algorithm which can be used with any **delay model** for the interconnect and transistor devices is
www.ee.rochester.edu:8080/~friedman/papers/TCASII.01.pdf

Proposal of a Timing Model for CMOS Logic Gates Driving a .. - Hirata, Onodera, Tamaru (1998) (Correct) (1 citation)
output waveform during input transition, **effective capacitance** is calculated by solving a non-linear Abstract We present a gate **delay model** of CMOS logic gates driving a CRC load for
www.tamaru.kuee.kyoto-u.ac.jp/~hirata/iccad98.ps.gz

Gate Load Delay Computation Using Analytical Models - Andrew Kahng (1996) (Correct) (1 citation)
A 2 2 A 3 C 2 =A 2 2 A 3 2) 2.3 **Effective Capacitance** Model The cell tables (or k-factor Thevenin equivalent model is a more effective **delay model** when the load is not purely capacitive, since
nexus6.cs.ucla.edu/~abk/papers/conference/c62.ps

Probabilistic Bottom-up RTL Power Estimation - Ferreira, Trullemans, al. (Correct)
have typically few parameters, namely an **effective capacitance** for each unit, a scaling factor in terms to compute the total power under the zero **delay model**. However, the ADD size grows up exponentially
www.dice.ucl.ac.be/~anmarie/CAD/ISQED_00.pdf

Try your query at: Google (CiteSeer) Google (Web) Yahoo! MSN CSB DBLP

CiteSeer Find: effective capacitance and delay an(Documents Citations

Searching for **effective capacitance and delay and model and interconnect**.
Restrict to: Header Title Order by: Expected citations Hubs Usage Date Try: Google (CiteSeer) Google (Web) Yahoo! MSN CSB DBLP
5 documents found. **Order: number of citations.**

Challenges and Opportunities for Design Innovations in Nanometer.. - Cong (1997) (Correct) (27 citations)
3) and derived the driver/buffer input **capacitance, effective** resistance, and intrinsic **delay** in each
capacitance, effective resistance, and intrinsic **delay** in each technology generation (shown in the
many challenges on **interconnect** performance, **model**ing, and reliability. It also drives the
cadlab.cs.ucla.edu/~cong/papers/src_report97_final.ps

One or more of the query terms is very common - only partial results have been returned. Try Google (CiteSeer).

Low-Power Architectural Synthesis and the Impact of.. - Mehra, Guerra, Rabaey (1996) (Correct) (10 citations)
DD is the supply voltage, and C eff is the **effective capacitance** switched. The C eff is in turn dependent
reductions, at the expense, however, of increased **delays**. A common approach to power reduction, therefore,
been integrated into the Hyper-LP system. A new **model** for estimation of bus power in partitioned
infopad.eecs.berkeley.edu/~renu/papers/vlsisp96.ps

New Efficient Algorithms for Computing Effective Capacitance - Andrew Kahng (1998) (Correct) (2 citations)
New Efficient Algorithms for Computing **Effective Capacitance** Andrew B. Kahng and Sudhakar Muddu
capacitance approach show that our resulting **delay** estimates are quite accurate -within 15% of
nexus6.cs.ucla.edu/~abk/papers/conference/c76.ps

Gate Load Delay Computation Using Analytical Models - Andrew Kahng (1996) (Correct) (1 citation)
A 2 2 A 3 C 2 =A 2 2 A 3 2) 2.3 **Effective Capacitance Model** The cell tables (or k-factor
Gate Load **Delay** Computation Using Analytical **Models** Andrew B.
nexus6.cs.ucla.edu/~abk/papers/conference/c62.ps

Improved Effective Capacitance Computations for Use in Logic.. - Kahng, Muddu (1999) (Correct)
Improved **Effective Capacitance** Computations for Use in Logic and Layout
capacitance approach show that the resulting **delay** estimates are quite accurate -within 15% of
vlsicad.cs.ucla.edu/papers/conference/c86.ps

Try your query at: Google (CiteSeer) Google (Web) Yahoo! MSN CSB DBLP

Published before October 2000
Terms used effective capacitance delay model

Found 31 of 109,693

Sort results by: relevance
Display results: condensed form
Save results to a Binder
Search Tips
Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 1 - 20 of 31 Result page: 1 2 next

Relevance scale

1 Buffer insertion with accurate gate and interconnect delay computation
Charles J. Alpert, Anirudh Devgan, Stephen T. Quay
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(118.92 KB) Additional Information: full citation, references, citings, index terms

2 Calculating worst-case gate delays due to dominant capacitance coupling
Florentin Dartu, Lawrence T. Pileggi
June 1997 **Proceedings of the 34th annual conference on Design automation - Volume 00**
Full text available: pdf(98.15 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

3 Interconnect design for deep submicron ICs
Jason Cong, Zhigang Pan, Lei He, Cheng-Kok Koh, Kei-Yong Khoo
November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(157.58 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

4 Simultaneous gate and interconnect sizing for circuit-level delay optimization
Noel Menezes, Satyamurthy Pullela, Lawrence T. Pileggi
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**
Full text available: pdf(82.95 KB) Additional Information: full citation, references, citings, index terms

5 TACO: timing analysis with coupling
Ravishankar Arunachalam, Karthik Rajagopal, Lawrence T. Pileggi
June 2000 **Proceedings of the 37th conference on Design automation**
Full text available: pdf(76.73 KB) Additional Information: full citation, abstract, references, citings, index terms

6 A gate-delay model for high-speed CMOS circuits
Florentin Dartu, Noel Menezes, Jessica Qian, Lawrence T. Pillage
June 1994 **Proceedings of the 31st annual conference on Design automation**
Full text available: pdf(253.28 KB) Additional Information: full citation, references, citings, index terms

7 Noise-aware repeater insertion and wire-sizing for on-chip interconnect using hierarchical moment-matching
Chung-Ping Chen, Noel Menezes
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(59.31 KB) Additional Information: full citation, references, citings, index terms

8 New efficient algorithms for computing effective capacitance
Andrew B. Kahng, Sudhakar Muddu
April 1998 **Proceedings of the 1998 international symposium on Physical design**

Full text available: pdf(711.21 KB) Additional Information: full citation, abstract, references, citings, index terms

9 Proposal of a timing model for CMOS logic gates driving a CRC &pgr; load
Akio Hirata, Hidetoshi Onodera, Keikichi Tamaru
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(684.15 KB) Additional Information: full citation, references, citings, index terms

10 Timing analysis and optimization of a high-performance CMOS processor chipset
U. Fassnacht, J. Schietke
February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(56.10 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

11 Power estimation for a submicron CMOS inverter driving a CRC interconnect load
Hung-Jung Chen, Bradley S. Carlson
March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**

Full text available: pdf(439.50 KB) Additional Information: full citation, abstract, references, index terms

12 Performance sensitivity analysis using statistical method and its applications to delay
Jing-Jia Liou, Angela Krstic, Kwang-Ting Cheng, Deb Aditya Mukherjee, Sandip Kundu
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**

Full text available: pdf(143.90 KB) Additional Information: full citation, references, citings

13 A sequential quadratic programming approach to concurrent gate and wire sizing
Noel Menezes, Ross Baldick, Lawrence T. Pileggi
December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(88.42 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

14 Critical path analysis using a dynamically bounded delay model
Soha Hassoun
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(787.75 KB) Additional Information: full citation, abstract, references, citings, index terms

15 FAR-DS: full-plane AWE routing with driver sizing
Jiang Hu, Sachin S. Sapatnekar
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(132.68 KB) Additional Information: full citation, references, citings, index terms

16 Static timing analysis taking crosstallk into account
Mattias Ringe, Thomas Lindenkreuz, Erich Barke
January 2000 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(62.37 KB) Publisher Site Additional Information: full citation, references, citings, index terms

17 Coping with RC(L) interconnect design headaches
Lawrence Pileggi
December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(96.33 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

18 RC interconnect synthesis—a moment fitting approach
Noel Menezes, Satyamurthy Pullela, Florentin Dartu, Lawrence T. Pillage
November 1994 **Proceedings of the 1994 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(794.71 KB) Additional Information: full citation, abstract, references, citings, index terms

19 An analytic calculation method for delay time of RC-class interconnects

W. K. Kal, S. Y. Kim
January 2000 **Proceedings of the 2000 conference on Asia South Pacific design automation**
Full text available: pdf(203.76 KB) Additional Information: full citation, references

20 IC analyses including extracted inductance models
Michael W. Beattie, Lawrence T. Pileggi
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**
Full text available: pdf(137.28 KB) Additional Information: full citation, references, citings, index terms

Results 1 - 20 of 31 Result page: **1** 2 next

Published before October 2000
Terms used effective capacitance delay model

Found 31 of 109,693

Sort results by relevance

Display results condensed form

Save results to a Binder

Search Tips

Open results in a new window

Try an Advanced Search
Try this search in The ACM Guide

Results 21 - 31 of 31 Result page: previous 1 2

Relevance scale

21 Timing metrics for physical design of deep submicron technologies
Lawrence Pileggi
April 1998 **Proceedings of the 1998 international symposium on Physical design**
Full text available: pdf(727.52 KB) Additional Information: full citation, abstract, references, citings, index terms

22 On switch factor based analysis of coupled RC interconnects
Andrew B. Kahng, Sudhakar Muddu, Egino Sarto
June 2000 **Proceedings of the 37th conference on Design automation**
Full text available: pdf(101.13 KB) Additional Information: full citation, abstract, references, citings, index terms

23 Transistor sizing in CMOS circuits
M. A. Cirit
October 1987 **Proceedings of the 24th ACM/IEEE conference on Design automation**
Full text available: pdf(380.83 KB) Additional Information: full citation, abstract, references, citings, index terms

24 Table-lookup methods for improved performance-driven routing
John Lillis, Premal Buch
May 1998 **Proceedings of the 35th annual conference on Design automation**
Full text available: pdf(271.81 KB) Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

25 Simultaneous buffer insertion and non-Hanan optimization for VLSI interconnect under a higher order AWE model
Jiang Hu, Sachin S. Sapatnekar
April 1999 **Proceedings of the 1999 international symposium on Physical design**
Full text available: pdf(773.78 KB) Additional Information: full citation, references, citings, index terms

26 Determination of worst-case aggressor alignment for delay calculation
Paul D. Gross, Ravishankar Arunachalam, Karthik Rajagopal, Lawrence T. Pileggi
November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**
Full text available: pdf(883.15 KB) Additional Information: full citation, references, citings, index terms

27 Planning for performance
Ralph H. J. M. Otten, Robert K. Brayton
May 1998 **Proceedings of the 35th annual conference on Design automation**
Full text available: pdf(301.86 KB) Additional Information: full citation, abstract, references, citings, index terms
Publisher Site

28 A multiple delay simulator for MOS LSI circuits
H. N. Nham, A. K. Bose
June 1980 **Proceedings of the 17th conference on Design automation**

Full text available: pdf(632.23 KB) Additional Information: full citation, abstract, references, citings, index terms

29 The Elmore delay as bound for RC trees with generalized input signals
Rohini Gupta, Byron Krauter, Bogdan Tutuianu, John Willis, Lawrence T. Pileggi
January 1995 **Proceedings of the 32nd ACM/IEEE conference on Design automation**

Full text available: pdf(244.03 KB) Additional Information: full citation, references, citings, index terms

30 Interconnect tuning strategies for high-performance ICs
A. B. Kahng, S. Muddu, E. Sarto, R. Sharma
February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(115.92 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

31 ClariNet: a noise analysis tool for deep submicron design
Rafi Levy, David Blaauw, Gabi Braca, Aurobindo Dasgupta, Amir Grinshpon, Chanlee Oh, Boaz Orshav, Supamas Sirichotiyakul, Vladimir Zolotov
June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(101.67 KB) Additional Information: full citation, abstract, references, citings, index terms

Results 21 - 31 of 31 Result page: previous 1 **2**

Results for "(effective capacitance<and>delay model<and>interconnect) <and> (pyr >= 1951 <..." e-mail printer friendly
Your search matched **29** of **1198558** documents.
A maximum of **100** results are displayed, **50** to a page, sorted by **Relevance** in **Descending** order.

1. **An analytical delay model for SRAM-based FPGA interconnections**
Zhou Feng; Huang Zhijun; Tong Jiarong; Tang Pushan;
Design Automation Conference, 1999. Proceedings of the ASP-DAC '99. Asia and South Pacific
18-21 Jan. 1999 Page(s):101 - 104 vol.1
Digital Object Identifier 10.1109/ASPDAC.1999.759723
AbstractPlus | Full Text: PDF(300 KB) **IEEE CNF**

2. **Interconnect simulation in a fast timing simulator ILLIADS-I**
Kutuk, H.; Goknar, I.C.; Kang, S.-M.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]
Volume 46, Issue 1, Jan. 1999 Page(s):178 - 189
Digital Object Identifier 10.1109/81.739264
AbstractPlus | References | Full Text: PDF(392 KB) **IEEE JNL**

3. **CMOS inverter current and delay model incorporating interconnect effects**
Hafed, M.; Rumin, N.;
Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on
Volume 6, 31 May-3 June 1998 Page(s):86 - 89 vol.6
Digital Object Identifier 10.1109/ISCAS.1998.705218
AbstractPlus | Full Text: PDF(324 KB) **IEEE CNF**

4. **Theory and algorithm of local-refinement-based optimization with application to device and interconnect sizing**
Cong, J.; Lei He;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 18, Issue 4, April 1999 Page(s):406 - 420
Digital Object Identifier 10.1109/43.752925
AbstractPlus | References | Full Text: PDF(452 KB) **IEEE JNL**

5. **Improved effective capacitance computations for use in logic and layout optimization**
Kahng, A.B.; Muddu, S.;
VLSI Design, 1999. Proceedings. Twelfth International Conference On
7-10 Jan. 1999 Page(s):578 - 582
Digital Object Identifier 10.1109/ICVD.1999.745217
AbstractPlus | Full Text: PDF(96 KB) **IEEE CNF**

6. **Table-lookup methods for improved performance-driven routing**
Lillis, J.; Buch, P.;
Design Automation Conference, 1998. Proceedings

15-19 Jun 1998 Page(s):368 - 373

AbstractPlus | Full Text: PDF(452 KB) IEEE CNF

7. **CMOS gate delay models for general RLC loading**
Arunachalam, R.; Dartu, F.; Pileggi, L.T.;
Computer Design: VLSI in Computers and Processors, 1997. ICCD '97. Proceedings., 1997 IEEE International Conference on
12-15 Oct. 1997 Page(s):224 - 229
Digital Object Identifier 10.1109/ICCD.1997.628872

AbstractPlus | Full Text: PDF(508 KB) IEEE CNF

8. **IEEE standard for integrated circuit (IC) delay and power calculation system**
IEEE Std 1481-1999
26 June 1999 Page(s):i - 390

AbstractPlus | Full Text: PDF(1780 KB) IEEE STD

9. **The Elmore delay as a bound for RC trees with generalized input signals**
Gupta, R.; Tutuianu, B.; Pileggi, L.T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 16, Issue 1, Jan. 1997 Page(s):95 - 104
Digital Object Identifier 10.1109/43.559334

AbstractPlus | References | Full Text: PDF(396 KB) IEEE JNL

10. **A sequential quadratic programming approach to concurrent gate and wire sizing**
Menezes, N.; Baldick, R.; Pileggi, L.T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 16, Issue 8, Aug. 1997 Page(s):867 - 881
Digital Object Identifier 10.1109/43.644611

AbstractPlus | References | Full Text: PDF(484 KB) IEEE JNL

11. **Clocking design and analysis for a 600-MHz Alpha microprocessor**
Bailey, D.W.; Benschneider, B.J.;
Solid-State Circuits, IEEE Journal of
Volume 33, Issue 11, Nov. 1998 Page(s):1627 - 1633
Digital Object Identifier 10.1109/4.726547

AbstractPlus | References | Full Text: PDF(172 KB) IEEE JNL

12. **High-level power modeling, estimation, and optimization**
Macii, E.; Pedram, M.; Somenzi, F.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 17, Issue 11, Nov. 1998 Page(s):1061 - 1079
Digital Object Identifier 10.1109/43.736181

AbstractPlus | References | Full Text: PDF(300 KB) IEEE JNL

13. **EWA: efficient wiring-sizing algorithm for signal nets and clock nets**
Kay, R.; Pileggi, L.T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 17, Issue 1, Jan. 1998 Page(s):40 - 49
Digital Object Identifier 10.1109/43.673631

AbstractPlus | References | Full Text: PDF(208 KB) IEEE JNL

14. **Short-circuit energy dissipation modeling for submicrometer CMOS gates**
Bisdounis, L.; Koufopavlou, O.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on]
Volume 47, Issue 9, Sept. 2000 Page(s):1350 - 1361
Digital Object Identifier 10.1109/81.883330

AbstractPlus | References | Full Text: PDF(280 KB) IEEE JNL

15. **A 2-GHz clocked AlGaAs/GaAs HBT byte-slice datapath chip**

Carlough, S.R.; Philhower, R.A.; Maier, C.A.; Steidl, S.A.; Campbell, P.M.; Garg, A.; Kyung-Suc Nah; Ernest, M.W.; Loy, J.R.; Krawczyk, T.W., Jr.; Curran, P.F.; Kraft, R.P.; Greub, H.J.; McDonald, J.F.;
Solid-State Circuits, IEEE Journal of
Volume 35, Issue 6, June 2000 Page(s):885 - 894
Digital Object Identifier 10.1109/4.845192

AbstractPlus | References | Full Text: PDF(748 KB) IEEE JNL

16. **Algorithms for non-Hanan-based optimization for VLSI interconnect under a higher-order AWE model**
Jiang Hu; Sapatnekar, S.S.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume 19, Issue 4, April 2000 Page(s):446 - 458
Digital Object Identifier 10.1109/43.838994

AbstractPlus | References | Full Text: PDF(360 KB) IEEE JNL

17. **Transient analysis of a CMOS inverter driving resistive interconnect**
Tang, K.T.; Friedman, E.G.;
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on
Volume 4, 28-31 May 2000 Page(s):269 - 272 vol.4
Digital Object Identifier 10.1109/ISCAS.2000.858740

AbstractPlus | Full Text: PDF(348 KB) IEEE CNF

18. **Exact output response computation of RC interconnects under polynomial input waveforms**
Gupta, S.; Patnaik, L.M.;
VLSI Design, 1999. Proceedings. Twelfth International Conference On
7-10 Jan. 1999 Page(s):160 - 163
Digital Object Identifier 10.1109/ICVD.1999.745142

AbstractPlus | Full Text: PDF(88 KB) IEEE CNF

19. **Spec-based repeater insertion and wire sizing for on-chip interconnect**
Menezes, N.; Chung-Ping Chen;
VLSI Design, 1999. Proceedings. Twelfth International Conference On
7-10 Jan. 1999 Page(s):476 - 482
Digital Object Identifier 10.1109/ICVD.1999.745201

AbstractPlus | Full Text: PDF(84 KB) IEEE CNF

20. **Proceedings Twelfth International Conference on VLSI Design. (Cat. No.PR00013)**
VLSI Design, 1999. Proceedings. Twelfth International Conference On
7-10 Jan. 1999
Digital Object Identifier 10.1109/ICVD.1999.745112

AbstractPlus | Full Text: PDF(448 KB) IEEE CNF

21. **Impact of crosstalk on delay time and a hierarchy of interconnects**
Yamashita, K.; Odanaka, S.;
Electron Devices Meeting, 1998. IEDM '98 Technical Digest., International
6-9 Dec. 1998 Page(s):291 - 294
Digital Object Identifier 10.1109/IEDM.1998.746357

AbstractPlus | Full Text: PDF(312 KB) IEEE CNF

22. **Proposal of a timing model for CMOS logic gates driving a CRC /spl pi/ load**
Hirata, A.; Onodera, H.; Tamaru, K.;
Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998 IEEE/ACM International Conference on
8-12 Nov 1998 Page(s):537 - 544

AbstractPlus | Full Text: PDF(548 KB) IEEE CNF

23. **Repeater and interconnect strategies for high-performance physical designs**
Muddu, S.; Sarto, E.; Hofmann, M.; Bashteen, A.;

Integrated Circuit Design, 1998. Proceedings. XI Brazilian Symposium on
30 Sept.-3 Oct. 1998 Page(s):226 - 231
Digital Object Identifier 10.1109/SBCCI.1998.715447

AbstractPlus | Full Text: PDF(80 KB) IEEE CNF

24. **Determination of worst-case aggressor alignment for delay calculation**
Gross, P.D.; Arunachalam, R.; Rajagopal, K.; Pileggi, L.T.;
Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998 IEEE/ACM International Conference on
8-12 Nov 1998 Page(s):212 - 219

AbstractPlus | Full Text: PDF(732 KB) IEEE CNF

25. **Getting to the bottom of deep submicron**
Sylvester, D.; Keutzer, K.;
Computer-Aided Design, 1998. ICCAD 98. Digest of Technical Papers. 1998 IEEE/ACM International Conference on
8-12 Nov 1998 Page(s):203 - 211

AbstractPlus | Full Text: PDF(992 KB) IEEE CNF

26. **Timing analysis and optimization of a high-performance CMOS processor chipset**
Fassnacht, U.; Schietke, J.;
Design, Automation and Test in Europe, 1998., Proceedings
23-26 Feb. 1998 Page(s):325 - 331
Digital Object Identifier 10.1109/DATE.1998.655876

AbstractPlus | Full Text: PDF(28 KB) IEEE CNF

27. **Interconnect tuning strategies for high-performance ICs**
Kahng, A.B.; Muddu, S.; Sarto, E.; Sharma, R.;
Design, Automation and Test in Europe, 1998., Proceedings
23-26 Feb. 1998 Page(s):471 - 478
Digital Object Identifier 10.1109/DATE.1998.655900

AbstractPlus | Full Text: PDF(92 KB) IEEE CNF

28. **Planning for performance**
Otten, R.H.J.M.; Brayton, R.K.;
Design Automation Conference, 1998. Proceedings
15-19 Jun 1998 Page(s):122 - 127

AbstractPlus | Full Text: PDF(568 KB) IEEE CNF

29. **Analytical fast timing simulation of MOS circuits driving RC interconnects**
Dharchoudhury, A.; Kang, S.M.;
VLSI Design, 1997. Proceedings., Tenth International Conference on
4-7 Jan. 1997 Page(s):111 - 116
Digital Object Identifier 10.1109/ICVD.1997.567971

AbstractPlus | Full Text: PDF(456 KB) IEEE CNF

[redacted]